

II. Amendment to the Claims

Claims 1-25 are pending in the present application. Of these, Claims 10-18 have been withdrawn and are canceled. Claims 6 and 23 have been amended as set forth below. New Claims 26-34 have been added. This version and listing of claims replaces all prior versions and listings of the claims.

1. (original) A metal-oxide-semiconductor (MOS) device, comprising:
 - a semiconductor layer of a first conductivity type;
 - a first source/drain region of a second conductivity type formed in the semiconductor layer;
 - a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region;
 - a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and
 - at least one contact, the at least one contact comprising:
 - a silicide layer formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate; and
 - at least one insulating layer formed directly on the silicide layer.
2. (original) The device of claim 1, wherein the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

3. (original) The device of claim 1, wherein substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer.

4. (original) The device of claim 1, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer.

5. (original) The device of claim 1, wherein the silicide layer forms a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer that are electrically isolated from the device.

6. (currently amended) The device of claim 1, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.

7. (original) The device of claim 1, wherein the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

8. (original) The device of claim 1, wherein the device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

9. (original) The device of claim 8, wherein the MOS device comprises a lateral DMOS (LDMOS) device.

10-18. (canceled)

19. (original) An integrated circuit (IC) device comprising a plurality of metal-oxide semiconductor (MOS) devices, at least one of the MOS devices comprising:

- a semiconductor layer of a first conductivity type;
- a first source/drain region of a second conductivity type formed in the semiconductor layer;
- a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region;
- a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and
- at least one contact, the at least one contact comprising:
 - a silicide layer formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate; and
 - at least one insulating layer formed directly on the silicide layer.

20. (original) The IC device of claim 19, wherein the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

21. (original) The IC device of claim 19, wherein substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer.

22. (original) The IC device of claim 19, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer.

23. (currently amended) The IC device of claim 19, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.

24. (original) The IC device of claim 19, wherein the device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

25. (original) The IC device of claim 19, wherein the silicide layer forms a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer that are electrically isolated from the device.

26. (new) A semiconductor device comprising a plurality of metal-oxide semiconductor (MOS) devices, at least one of the MOS devices comprising:

a semiconductor layer of a first conductivity type;

a first source/drain region of a second conductivity type formed in the semiconductor layer;

a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region;

an implant region of the first conductivity type formed at least adjacent an upper surface of said semiconductor layer and at least laterally adjacent and contacting said first source/drain

region, said implant region extending laterally in a direction opposite the second source/drain region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions;

at least one contact, the at least one contact comprising a silicide layer formed on and in electrical connection with at least a portion of the first source/drain region and said implant region, the silicide layer extending laterally away from the gate and forming a substantially low-resistance electrical path in parallel with an electrical path between the first source/drain region and the implant region, wherein substantially all current associated with the first source drain region passes through the silicide layer in a direction from the first source/drain region to a portion of said implant region proximate the upper surface of said semiconductor layer; and

at least one insulating layer formed directly on the silicide layer.

27. (new) The device of claim 26, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer.

28. (new) The device of claim 26 wherein said semiconductor layer is formed over a semiconductor substrate, said device further comprising a trench sinker electrically coupling said implant region to said substrate.

29. (new) The device of claim 28, wherein said trench sinker comprises an implant sinker.

30. (new) The device of claim 26, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain

region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.

31. (new) The device of claim 26, wherein the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

32. (new) The device of claim 26, wherein the device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

33. (new) The device of claim 32, wherein the MOS device comprises a lateral DMOS (LDMOS) device.

34. (new) The device of claim 26, wherein said silicide contact has a thickness of less than or equal to about 0.1 μm .